Terms used **claudionor multiple time frame** Found **4** of **151,219**

Sort results by relevance

Display results expanded form

Save results to a Binder

Search Tips

Open results in a new window

Try an Advanced Search

Try this search in The ACM Guide

Results 1 - 4 of 4

Relevance scale

1 Synthesis from mixed specifications

G. De Micheli, V. Mooney, C. Coelho, T. Sakamoto

September 1996 **Proceedings of the conference on European design automation**

Full text available: pdf(347.62 KB) Additional Information: full citation, references, citings, index terms

2 Dynamic scheduling and synchronization synthesis of concurrent digital systems under system-level constraints

Claudionor N. Coelho, Giovanni De Micheli

November 1994 **Proceedings of the 1994 IEEE/ACM international conference on Computer-aided design**

Full text available: pdf(783.93 KB) Additional Information: full citation, abstract, references, citings, index terms

We present in this paper a novel control synthesis technique for system-level specifications that are better described as a set of concurrent synchronous descriptions, their synchronizations and constraints. The proposed synthesis technique considers the degrees of freedom introduced by the concurrent models and by the environment in order to satisfy the design constraints.Synthesis is divided in two phases. In the first phase, the original specification is translated into an alg ...

3 Synthesis of low-power selectively-clocked systems from high-level specification

L. Benini, P. Vuillod, G. de Micheli, Claudionor Coelho

November 1996 **Proceedings of the 9th International Symposium on System Synthesis**

Full text available: pdf(1.06 MB) Publisher Site Additional Information: full citation, abstract

In this paper we propose a technique for synthesizing low-power systems from a high-level specification. We analyze the control flow of the specification to detect mutually exclusive sections of the computation. A selectively-clocked interconnection of interacting FSMs is automatically generated and optimized where each FSM controls the execution of one section of computation. Only one of the interacting FSMs is active at any given clock cycle, while all the others are idle and their clock is

st ...

Keywords: High level synthesis, low power, finite state machines, gated clocks.

4 Verification (co-organized with LA-TTTC): Exception handling in microprocessors using assertion libraries

Fernando Cortez Sica, Claudionor N. Coelho, José Augusto M. Nacif, Harry Foster, Antônio Otávio Fernandes

September 2004 **Proceedings of the 17th symposium on Integrated circuits and system design**

Full text available: pdf(237.87 KB) Additional Information: full citation, abstract, references, index terms

In complex System-on-a-Chip (*SoC*) designs, designers often need to add new features into an original processor core, such as to extend the exception handling mechanism to consider exceptions in the remaining portion of the *SoC* design. We present in this paper a scalable architecture that can be used to add complex exception handling mechanisms in processor cores and how it can be used to extend the fixed set of exceptions found in microprocessor cores. This mechanism is based on th ...

Keywords: assertions, exceptions handling

Results 1 - 4 of 4